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10/804,713	03/18/2004	Chao-Hsiang Yang	67,200-967	7508

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,713	YANG, CHAO-HSIANG	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-14,16-26 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-14,16-26 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 11/01/2005 forms the basis for his office action. In said Amendment Applicant substantially amended all previously pending claims as well as the specification, paragraphs [0003], [0004] and [0005], and added a new claim 28. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Information Disclosure Statement

From said Amendment examiner concludes that indeed Applicant has meant to make of record through the IDS patent to Ying et al (6,300,252).

Specification

The amendment to paragraph [0003] in the specification is objected to as it fails to show any difference between the original specification and the amendment.

The amendment to paragraph [0004] is herewith accepted and removes an objection in this regard made in the previous office action (page 2).

The specification is, however, objected to with regard to paragraph [0005] as amended because the phrase "The fuse windows were openings are then selectively etched..." contains two main verbs in one main sentence ("were" and "are" and hence is incomprehensible.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claim 18*** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. In particular, topmost metallization layer 64 is NOT disclosed to be copper (Figure 2) while, although the lower part of 12 in Figure 3 qualifies as the claimed copper island, disposed in a low dielectric material inter-metal dielectric layer for which only 28 is a match, no etch stop layer on upper and lower main surface of 28 is disclosed. Therefore, no embodiment by Applicant discloses claim 18 as amended.

2. ***Claims 19 and 21*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. In particular, within the context of the claimed copper island Figure 3 is the only embodiment disclosed by Applicant while no dielectric layer on said passivation layer is disclosed within the context of the second embodiment. Hence claim 19, and by dependence claim 21, lack disclosure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1-5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata (6,433,406 B1) (previously made of record) in view of Huang et al (6,121,073) as made of record by IDS.

Kagiwata teaches a semiconductor device fuse structure (title, abstract, columns 5-8 and Figures 3-5) comprising:

a substrate 1 (col. 5, line 52) (Fig. 3B);

a top inter-wiring dielectric layer 3 on said substrate (Fig. 3B);

at least two top *wiring* lines 4/6 and 5/6, respectively, (column 4, lines 59-63) in said top inter-*wiring* dielectric layer, said at least two top *wiring* lines comprising a topmost *wiring* layer (6 in each) (column 5, line 62) in electrical communication with at least one lower *wiring* layer 4 and 5, respectively, (column 5, lines 59-62) comprising a first *wiring* layer (both 4 and 5 are *wiring* layers (lco.cit.));

a fuse 2 (column 5, lines 52-53) on said top inter-*wiring* dielectric layer, said fuse providing electrical communication between said at least two top *wiring* lines by spanning a distance between said at least two top *wiring* lines (Figure 3B); a protective layer (column 6, lines 7-10) on said fuse; and

a window (between grooves 7) formed through a thickness portion of the protective layer (column 5, line 64 – column 6, line 10; note that 8 covers the entire lateral portion illustrated in Figure 3B).

Kagiwata does not necessarily teach the limitation that said at least two top wiring lines are metal lines. However, it would have been obvious to include said limitation in view of Huang et al, who, in a patent on a method of making a fuse structure teach the selection of metal for said wiring lines (22 and 26 left and right in Figure 3, corresponding to wiring lines 4/6 and 5/6 of Katigawa, respectively) (see column 6, line 7 and line 24). *Motivation* to include the teaching by Huang in this regard derives from the high conductivity of metal, making it the material of choice for wiring for the purpose of electrical conduction.

Finally, the pre-amble limitation "to prevent dielectric layer cracking at corner portions of associated metallization structures", aside from not being in the bulk of the claim, constitutes functional language. Applicant is reminded that while features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

On claim 2: said protective layer on said fuse comprises a dielectric layer (both 10a and 10b are dielectric layers: see column 8, lines 10-33).

On claim 3: said dielectric layer (through 10a) comprises silicon dioxide.(column 8, line 23).

*On claim 4:*said fuse comprises aluminum (Al) (column 5, lines 52-53).

On claim 5: in the combined invention said at least two top metal lines comprise copper (cu) (through the teaching of the material selection of Al/Cu for element 22: col. 6, lines 6-7 in Huang).

2. ***Claims 6, 9 and 11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata (6,433,406 B1) in view of Kajita et al (JP02001093981A) (previously made of record) and Huang et al (6,121,073) (as made of record in IDS).

Kagiwata teaches as conventional art (title, abstract, Figures 1-2, columns 1-3 and col. 5, lines 49-53) a semiconductor device comprising:

two separated and respectively interconnected wiring structures each extending through a plurality of low-dielectric material interconnected wiring structures 106 and 107, respectively, (column 1, lines 35-36) and a low dielectric material inter-wire dielectric material dielectric layers (portions of 109 surrounding the structure 106/108 and 107/108, respectively) (column 1, lines 35-36); and wherein a fuse 102 (column 2, lines 29-39) extends between each of the interconnected wiring structures in an uppermost inter-wire dielectric layer; and

a window 110 (as defined with indentations marking its frame as shown in Figure 1B) is disposed over a top portion of said fuse, said window extending through a thickness portion of a silicon dioxide layer 109 (portion on said fuse; Figure 1B; column 3, lines 35-36) on said fuse.

Kagiwata does not necessarily teach interconnected wiring structures to be metallization structures. However, it would have been obvious to include said limitation in view of Huang et al, who, in a patent on a method of making a fuse structure teach the selection of metal for said interconnected wiring structures (22 and 26 left and right in Figure 3, corresponding to wiring structures 106/108 and 107/108 of Katigawa, respectively) (see column 6, line 7 and line 24).

Motivation to include the teaching by Huang in this regard derives from the high conductivity of metal, making it the material of choice for wiring for the purpose of electrical conduction.

Kagiwata does not necessarily teach the limitation that the interconnected wiring structures comprise copper (and hence be metallization structures) and the fuse to comprise aluminum. However, it would have been obvious to include sadi limitation in view of Kajita et al, who, in a patent on a semiconductor device with a fuse (see title and English abstract), - hence closely related art, teach to select said two top wiring lines to comprise copper (and hence be metallization layers) (see English abstract, "Solution") while forming the fuse of aluminum (loc.cit.) so as to prevent fuse material to diffuse into the semiconductor device, in particular transistors on a substrate.

Motivation to include the teaching by Kajita et al derives from the application also of Kagiwata to transistors, being part of DRAM's (column 1 of Kagiwata). Combination merely involves a particular sub-selection of materials already recommended by Kagiwata (see Kagiwata, col. 5, lines 49-54).

On claim 9: in the combined invention each of the metallization structures include a first metal layer 106 or 107, respectively, and a topmost metal layer 108, each of said topmost metal layers 108 connected to said fuse (column 1, lines 34-36).

On claim 11: the semiconductor device further comprises a plug 105 (col. 1, l. 57-59) extending between the first metal layer and the topmost metal layer of the structure.

1. ***Claim 10*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagitawa, Kajita et al and Huang et al as applied to claim 9 above, and further in view of Ying et al (6,300,252 B1) (as made of record in IDS). As detailed above, claim 9 is unpatentable over Kagiwata in view of Kajita et al and Huang et al, neither necessarily teaching the further limitation as defined by claim 10. However, the term "etch stop layer" in the present context of the device invention contains functional language to the extent in which purpose for etching rather than material constitution is indicated by said term. Applicant is reminded in this regard that in reference to the claim language, such as in the present claim, referring to "etch stop", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the

claim. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). For this reason patentable weight is only given to the term "etch stop layer" for the material constitution implied by the term in view of the specification (page 11, discussing silicon nitride layer 54 as "etch stop" layer), and not for the purpose of providing an etch stop. In this context it would have been obvious to include silicon nitride layers on each upper and lower face of said inter-metal dielectric layer (said portion of 109 comprising low-k dielectric material interposed between said first and second metal layers) in view of Ying et al, who, in a patent on etching fuse windows for a semiconductor device (title and abstract), hence closely related art, teach to include a silicon nitride layer 72 (col. 6, l. 55-63) on an upper main face of low-k dielectric layer 60/66/70 (TEOS, e.g.) (note that 60/66/70 does comprise said low-k dielectric material interposed between metal layers M1, M2 or M3 on the one hand and M4 on the other hand) so as to prevent moisture penetration (col. col. 6, l. 63) and a silicon nitride layer 54 on a lower main face of said low-k dielectric layer so as to function as an etch stop layer (col. 6, l. 18-26). *Motivation* to include the teaching by Ying et al in this regard derives immediately from the generic undesirability of moisture as conducting material in a fuse for layer 72 and from the need to conduct an etching step (as described in Ying in col. 7, l. 35-40) also in Kagiwata (col. 7, l. 8-17).

2. ***Claim 12*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata, Kajita et al and Huang et al as applied to claim 6 above, and further in view of Admitted Prior Art by Applicant. Neither Kagiwata nor Kajita et al nor Huang et al necessarily disclose a thickness or thickness range for said aluminum fuse. However, it

would have been obvious to include the further limitation on the range of the thickness of the fuse in view of Admitted Prior Art by Applicant (page 3), who teach a range between 500 Å and 5000 Å, which range overlaps with the range as claimed (1000-7000 Å). Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson, 65 USPQ2d 1379 (CA FC 2003).*

3. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata, Kajita et al and Huang et al as applied to claim 9 above, and further in view of Liaw (6,255,715) (previously made of record). As detailed above, claim 9 is unpatentable over Kagiwata in view of Kajita et al and Huang et al, none necessarily teaching the further limitation as defined by claim 13. *However, it would have been obvious to include said further limitation in view of Liaw et al,* who, in a patent on a fuse with guard ring for a semiconductor device or integrated circuit (title, abstract and col. 1, l. 5-18), hence closely related to the art of Kagiwata, teach the thickness of the topmost metal layer 54 to be in the range of between about 2000 and 8000 Å (col. 6, l. 25-30). *Applicant is reminded* that it has been held that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

4. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajita et al (JP02001093981 A) in view of Omura et al (US 2004/0012073 A1).

Kajita et al teach a semiconductor device including (cf. English abstract, Description of the Drawings and par. [0044] in the computerized translation and Figures 2) a fuse 5/6 comprising a first layer 2/4/5 comprising a copper island 5 disposed in a dielectric material inter-metal dielectric layer 2 and a second layer 6/8/9 over the first layer, and wherein the second layer comprises aluminum; and a fuse window 16 disposed over said second layer, said fuse window extending through a thickness portion of at least one dielectric layer (low-k dielectric 9) (see [0039]; SiO:F) overlying said fuse.

Kajita et al do not necessarily teach the limitation that said dielectric material inter-metal dielectric layer 2 to be a low dielectric layer (i.e., have a low value of the dielectric constant).

However, it would have been obvious to include said limitation in view of Omura et al, who, in a patent application drawn to a semiconductor device with fuse (title, abstract), hence analogous art, teach both dielectric layers 13 and 19, corresponding to layers 2 and 9, respectively, to be made of the same low-k dielectric material, namely: TEOS (see paragraphs [0047] and [0051]) so as to shorten the delay in the fuse action (see [0007]).

Motivation to include the teaching by Omura et al in the invention by Kajita et al derives at least from the simplification resulting from using the same material for both dielectric layers.

5. ***Claim 16*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajita et al and Omura et al as applied to claim 14 as shown above, and further in view of Ying et al (6,300,252) (made of record in IDS). *As detailed above, claim 14 is unpatentable over Kajita et al in view of Omura et al. Kajita et al nor Omura et al necessarily teach the further limitation that said at least one dielectric layer comprises a passivation layer on the second layer, said passivation layer comprising silicon dioxide. However, it would have been obvious to include said further limitation of claim 16 in view of Ying et al,* who, in a patent on a method of making a semiconductor device with fuse (abstract), hence closely related art, teach that the fuse window opening is made by etching through a passivation layer 72/74 using a first etchant and etching the opening through the inter-metal dielectric layers (60,66,70) using a second etchant, wherein the first etchant has low selectivity to the material of the passivation layer, thereby increasing control over the etching process and thus create a superior quality fuse (see column 7, lines 5-35 and Figures 4-5). *Motivation* for inclusion of the teaching by Ying et al in this regard derives from the superior fuse quality obtained by the two-step etching process as explained by Ying et al.

6. ***Claims 17 and 20*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajita et al and Omura et al as applied to claim 14 above, and further in view of Shimooka et al (JP 11224900 A).

As detailed above, claim 14 is unpatentable over Kajita et al in view of Omura et al. Neither Kajita et al nor Omura et al necessarily teach the further limitation defined by claim 17.

However, it would have been obvious to include said limitation in view of Shimooka et al, who, in a patent on semiconductor device with fuse (title, abstract, and "Field of the Invention", column 1), hence analogous art, teach a dual damascene structure 8CD of a multilayered copper dual damascene wiring including copper island 11 and barrier metal 3 and a barrier metal 9, thus teaching a first metal layer 6CD and a topmost metal layer 8CD comprising the copper island and wherein the inter-metal dielectric layer 7 (see Description of the Drawings) is interposed between the first metal and the topmost metal layer (see English abstract and Drawing 1).

Motivation to include the teaching by Shimooka et al in the invention derives from the protection of the underlying device components provided by said damascene structure as explained by Shimooka et al (see English abstract, "Solution").

On claim 20: per definition, a "dual damascene" structure, is a multi-level metal interconnect system with vias connecting the respective levels vertically; see, e.g., Wolf et al, ISBN0-9616721-6-1, pages 798-799. The via connecting 6CD with 8CD meets the claim limitation on plug.

7. ***Claims 22-26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kagiwata and Huang et al as applied to claim 1 and further in view of Kajita et al and Pricer et al (6,335,229 B1) (see IDS).

On claim 22: The semiconductor device defined by the above-stated combination of Kagiwata and Huang et al as delineated above in the rejection of claim 1 can be used and is advocated to be used (Kagiwata col. 1, l. 40-55 and Figure 1D) as a method of

blowing a fuse in a semiconductor device, said device including at least a first metallization layer 106/107 comprising copper being obvious through the specific teaching by Kajita et al as discussed overleaf in this section), and a fuse comprising aluminum (again rendered obvious through the specific teaching by Kajita et al as explained overleaf in this section).

Neither Kagiwata nor Kajita et al necessarily limit the range of the wavelength as claimed. However, as shown by Pricer et al, a range between 150 nm and 400 nm is conventional for blowing fuses through low-k dielectric material (col. 4, l. 47-56). Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case said ranges clearly and substantially overlap.

On claim 23: the protective layer of Kagiwata further includes a fuse passivation layer 110 (col. 1, l. 37-39).

On claim 24: Kagiwata further teaches that the inclusion of a silicon dioxide layer between a silicon nitride layer and the fuse reduces the mechanical stress between said fuse and said silicon nitride layer (col. 8, l. 11-33).

On claims 25-26: an upper face of the fuse by Kagiwata comprises aluminum (col. 5, lines 52-53). Furthermore, in the combined invention inclusive of the teaching by Huang et al the two top metal lines comprise copper (col. 6, liners 5-10). In addition, as

already discussed overleaf, Kajita et al, in a patent on a semiconductor device with a fuse (see title and English abstract), - hence closely related to the art of Kagiwata, teach to select said two top metal lines to comprise copper, each forming a copper island (see English Abstract, "Solution") while forming the fuse of a first layer of aluminum (loc.cit.) so as to prevent fuse material to diffuse into the semiconductor device, in particular transistors on the substrate (claim 25); alternatively the copper island defined above can be considered part of the fuse, thus meeting claim 26, as then the second layer is above-mentioned first layer of aluminum. *Motivation* to include the teaching by Kajita derives from the application also of Kagiwata to transistors, being part of DRAMs (col. 1 of Kagiwata). *Combination* merely involves a particular sub-selection of materials already recommended by Kagiwata (see Kagiwata, col. 5, l. 49-54).

8. ***Claim 28*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Castagnetti et al (6,828,653 B1) in view of Pricer (6,335,229 B1) (see IDS).

Castagnetti et al teach a method of blowing a fuse structure (title, abstract, Figures 2 and 3, particularly Figure 2F; columns 4-7) capable to operate without low-dielectric material layer cracking at corner portions of associated metallization structures, said fuse structure comprising:

a fuse window (column 7, lines 7-11) formed through at least one dielectric layer (otherwise thicker existing portion of 238) (Figure 2F) overlying an upper face of an aluminum fuse 230 (column 6, lines 30-43) to expose a passivation layer 238 (col. 6, lines 46-60) comprising silicon dioxide (column 6, lines 49-50) on said fuse (Figure 2F),

said fuse window selectively disposed over said upper face of said aluminum fuse 230 (Figure 2F);

said aluminum fuse spanning a distance between two copper metallization structures 211 (column 5, lines 30-40), each of said copper metallization structures comprising interconnected damascene structures (column 5, lines 34-37) extending through a plurality of low dielectric material layers (loc.cit.);.

wherein said method comprises:

directing a laser beam (col. 6, line 66 – col. 7, line 11) onto said fuse through said silicon dioxide passivation layer (loc.cit.)

Castagnetti et al do not necessarily teach using a laser wavelength ranging from 300-500 or 1000-1400 nm.

However, as shown by Pricer et al, a range between 150 nm and 400 nm is conventional for blowing fuses through low-k dielectric material (col. 4, l. 47-56). Applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003). In the underlying case said ranges clearly and substantially overlap.

Response to Arguments

Applicant's arguments filed 11/01/05 have been fully considered but they are not persuasive. In particular, examiner appreciates amendments that overcome the claim

objections for minor informalities and specification, except for a cryptic lack of any amendment in "amended portion" [0003] of the specification, and a persistent problem with [0004] indicated overleaf, while it is noted that claim 27 has been cancelled; the double patenting rejection of claim 27 has thus been overcome. All arguments in traverse are formulated in terms of blanket statements that the prior art as cited does not teach certain paragraphs of the newly amended claim language. The above rejections show, however, that with some exceptions this is in error. The language of the present rejections, given here for the first time possible, is herewith incorporated in this "Response to Arguments". New prior art has been cited to supplement wherever needed.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
January 3, 2005

MATTHEW LUU
PRIMARY EXAMINER